# EE 4350: Experiment 5

# Spring 2025

# Two Stage Op Amp Design

## Introduction

In many applications of operational amplifiers, the gain of a single-stage amplifier is not adequate. Operational amplifier architectures that use two or more gain stages are widely used when higher gains are needed. Additional phase shift is invariably introduced when multiple gain stages are cascaded and compensation of these structures is invariably required to maintain acceptable magnitude response or time-domain response of feedback circuits that use the multiple-stage architectures. Of the multiple-stage architectures that are used, two-stage configurations are the most popular because primarily of the challenges associated with compensating three or more stages. In this experiment, a two-stage op amp using the basic architecture shown in Fig. 1 will be designed. Though shown with n-channel inputs on the first stage and p-channel inputs on the second stage, you may use either n-channel or p-channel inputs. After the initial two-stage design is completed, the right half-plane zero will be removed.

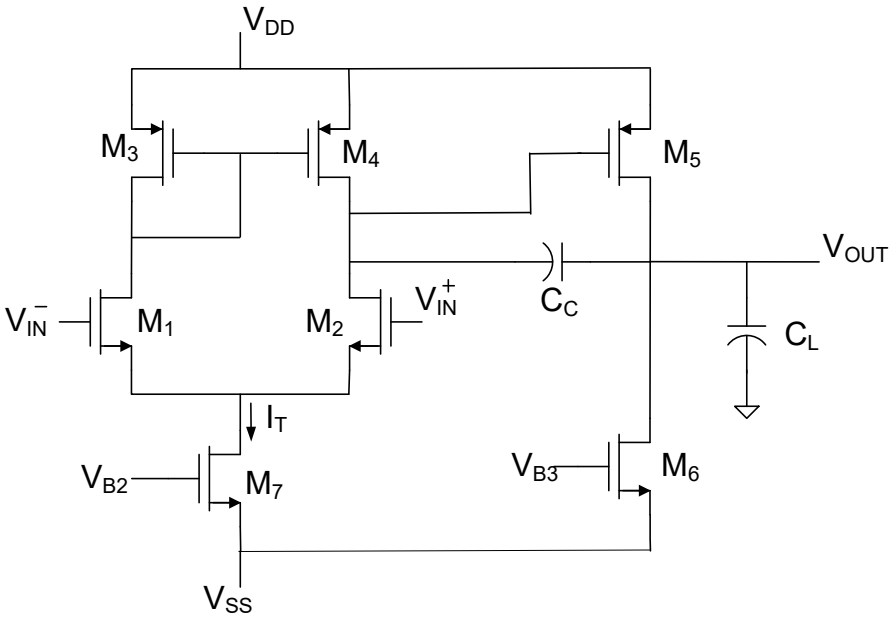


**Fig. 1 Basic Two-Stage 7T Miller Compensated Amplifier**

Part 1: **Design a two-stage operational amplifier using the architecture of Fig. 1 that meets the following specifications while keeping the power as small as possible:**

- 3.3 V power supply (±1.65V)
- $C_L$ = 20pF
- All components from the TSMC 0.18µ CMOS process (except for the 4 ideal voltage sources $V_{DD}$, $V_{SS}$, $V_{B2}$, $V_{B3}$)
- Typical $V_{CM}$ = 0V (use this if in doubt when running simulations)
- DC gain ≥ 60 dB
- GB ≥ 2.5 MHz
- Compensation for near maximum closed-loop bandwidth without overshoot in magnitude response with unity-gain feedback (β=1)
- Systematic offset voltage ≤ 10mV

- Input common-mode range (ICMR) that includes the interval [-0.4V, 0.4V]
- Output signal swing range that includes the interval [-0.4, 0.4]
- A Random Offset Voltage (3 sigma value) of at most 20mV

When you start design, identify the degrees of freedom you have, the constraints, and **specify explicitly how you will use the degrees of freedom available in your design**. When achieving near maximum closed-loop bandwidth for the power you consume, pay specific attention to how you partition power between the two stages.

The compensation criteria may appear a bit unusual so a bit of rationale will be given. The closed-loop pole Q for maximum bandwidth without overshoot will be about 0.707. So if you are comfortable with determining the closed-loop pole Q, you can target a closed-loop Q of 0.707. But if you can not readily obtain the pole Q during compensation, the following is a strategy you may consider following for compensation. If your amplifier is over-compensated you will not see overshoot but the bandwidth for the power you allocate will not be near maximum. So you may want to initially compensate your amplifier for maybe 4dB of gain peaking. That would correspond to a pole Q of around 1.25 Then increase the compensation capacitor just enough to eliminate the gain peaking. Since the compensation capacitor for this structure is proportional to $1/Q^2$, you will need to increase the compensation capacitor around about a factor of 3 to drop the pole Q from 1.25 to .707.

The design should include a complete circuit schematic and Spectre simulation results that compare analytical performance with simulated results. (**This means you should include analytical predictions of the performance, as well as simulation results, and commentary on the differences in your report).**

A layout of the circuit is not necessary.

Report the following performance of the amplifier:

- DC Gain
- GB
- ICMR
- Systematic input offset voltage
- Expected 3 sigma input offset voltage value
- SR
- Output signal swing range
- Quiescent power consumption
- Pole Zero plot with the dominant poles marked in the open loop and closed loop (unity gain) configurations
- Pole Q in the unity gain feedback configuration
- Magnitude response of the amplifier in a unity gain feedback configuration
- Phase Margin in the unity gain feedback configuration
- Signal to Noise Ratio (SNR) at the output if a 500mV p-p sinusoid is applied to the input in a unity gain feedback configuration

## Part 2: **Design of a two-stage operational amplifier using the architecture of Fig. 1 modified to remove the RHP zero**

In this design, move the RHP zero of the previous design to the LHP to cancel the non-dominant pole. After moving the zero, change the compensation capacitor to again get maximum closed-loop bandwidth for the power allocated. Compare the performance of the modified op amp with that of the original op amp.

## Extra Credit: **Use a Monte Carlo simulation to determine the 3σ input offset voltage**

Run the systematic input offset voltage simulation using a Monte Carlo simulation with 200 iterations. Report the 3σ offset voltage value and the offset voltage histogram.